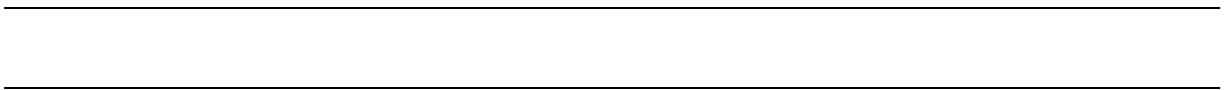




**CONNECTOR PERFORMANCE STANDARD
FOR OUTLINES OF SOLID STATE AND
RELATED PRODUCTS**

**PS-007
LPDDR5 CAMM2 Connector
Performance Standard**



JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

**Date: July 2024
Item: 11.14-225a**

Issue: A

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LPDDR5 CAMM2 Connector Performance Standard

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LPDDR5 CAMM2 Connector Performance Standard

(From JEDEC Board Ballot JCB-15-30, formulated under the cognizance of the JC-11.14 Subcommittee on Microelectronic Assemblies.)

1 Scope

This standard defines the form, fit and function of LPDDR5 CAMM2 connectors to support channels with transfer rates beyond 6.4 GT/S. It contains mechanical, electrical and reliability requirements for connector mated to a module with nominal thickness of 1.20 mm. The intent of this document is to provide performance standards to enable connector, system designers and manufacturers to build, qualify and use the LPDDR5 CAMM2 connectors in client platforms.

1.1 Connector Overview

LPDDR5 CAMM2 connector is a compress-mount technology (CMT) connector, retention is needed to ensure the function of the 1.38 mm X 1.0 mm pitch connector, which is defined for applications where a 1.20 mm nominal thickness CAMM2 module card mounted over the connector, parallel to the system board.

2 References

The following references provide normative requirements as specified in the body of this document:

- JEDEC MO-357: LPDDR5 CAMM2, 1.38 mm x 1.00 mm Pitch Microelectronic Assembly
- JEDEC SO-032: Plastic Dual Upper to Bottom, 1.38 mm x 1.00 mm Pitch Connector (CMT)
- EIA-364-1000: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment
- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-09: Durability Test Procedure for Electrical Connectors and Contacts
- EIA-364-13: Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23: Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
- EIA-364-27: Shock Test Procedure for Electrical Connectors
- EIA-364-28: Vibration Test Procedure for Electrical Connectors and Sockets
- EIA-364-29: Contact Retention Test Procedure for Electrical Connectors
- EIA-364-31: Humidity Test Procedure for Electrical Connectors and Sockets
- EIA-364-32: Thermal Shock Test Procedure for Electrical Connectors and Sockets
- EIA 364-70: Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- JEDEC JESD22-B108: Coplanarity Test for Surface-Mount Semiconductor Devices
- JS709A Defining "Low-Halogen" Electronic Products

3 Acronyms, terms, and definitions

Table 1 - Terms and Definitions

Term	Description
BOL	Beginning of Life
dB	Given in dB-volts, i.e., $20\log_{10}(V_2/V_1)$
CAMM2	Compression Attached Memory Module 2
CMT	Compressed Mount Technology
DUT	Device under test
EIA	Electronics Industry Alliance
EOL	End of Life
JEDEC	JEDEC Solid State Technology Association
LPDDR5	Low Power Double Data Rate 5
System board	PCB on which the DDR5 connector is mounted

4 Pin Numbering

This section describes pin numbers in LPDDR5 CAMM2 connector. The LPDDR5 CAMM2 connector pin number is shown in Figure 1

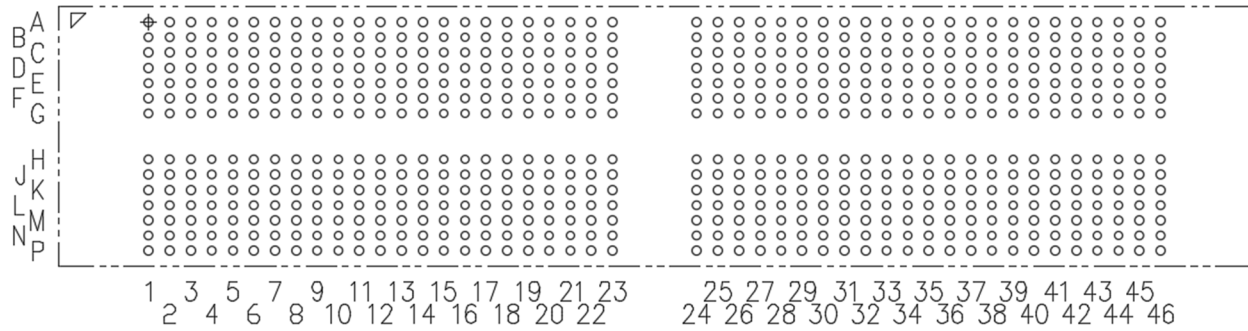


Figure 1 LPDDR5 CAMM2 Connector Number Sequence

5 Connector Socket Outline

5.1 LPDDR5 CAMM2 Connector Overview

A primary consideration for LPDDR5 CAMM2 development is to support modular LPDDR5 solution, rather than relying solely on soldered LPDDR5 memory on the motherboard.

To encourage widespread adoption of LPDDR5 CAMM2, the connector and module form factor is aligned with DDR5 SODIMM standards and keep the connector and module length at a maximum of 78 mm. The connector height should be kept at 1.0 mm nominal to minimize the overall height of the LPDDR5 CAMM2 solution.

The LPDDR5 CAMM2 connector features three posts, with two serving as alignment features and the third providing guidance to improve serviceability. The connector also includes six mounting holes, but only the three holes located at the center in the width direction are used for LPDDR5 CAMM2 retention. The other three holes, located near the edge, are reserved for other applications.

5.2 Socket outline

A general view of the LPDDR5 CAMM2 connector is shown in Figure 2. The socket outlines are shown in Figure 3. All dimensions are in millimeters.

For the detailed outline, refer to JEP95, SO-032, variation CAxx

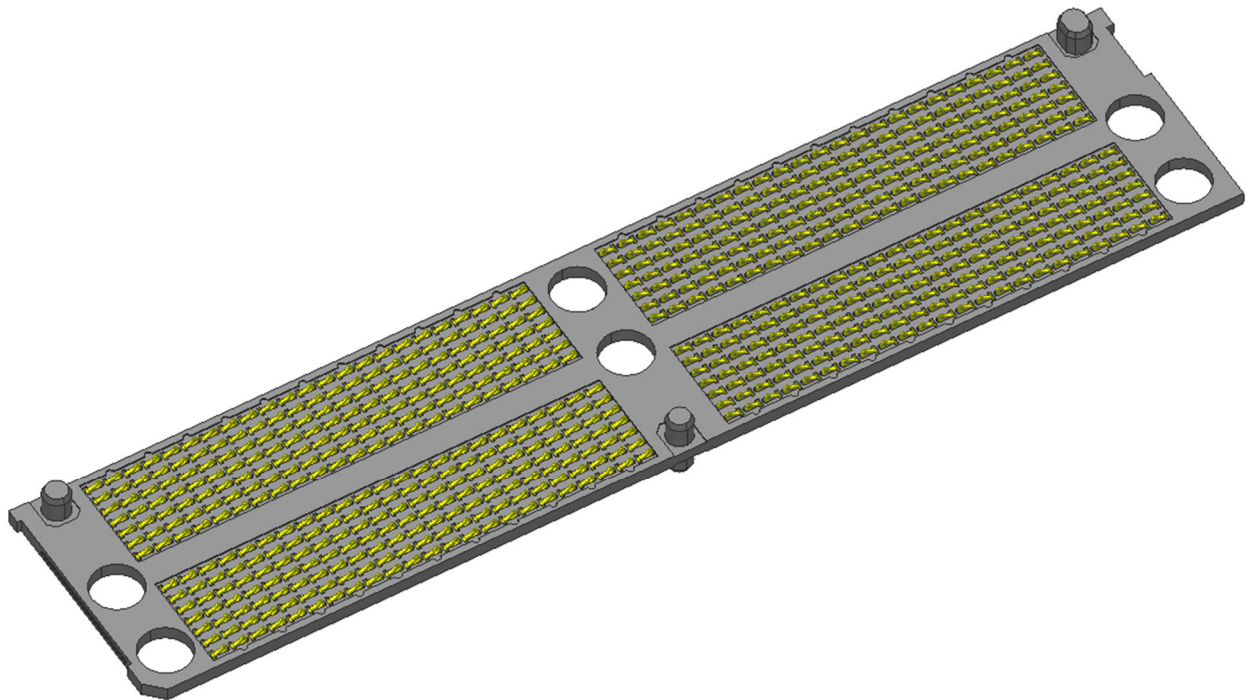


Figure 2 LPDDR5 CAMM2 connector

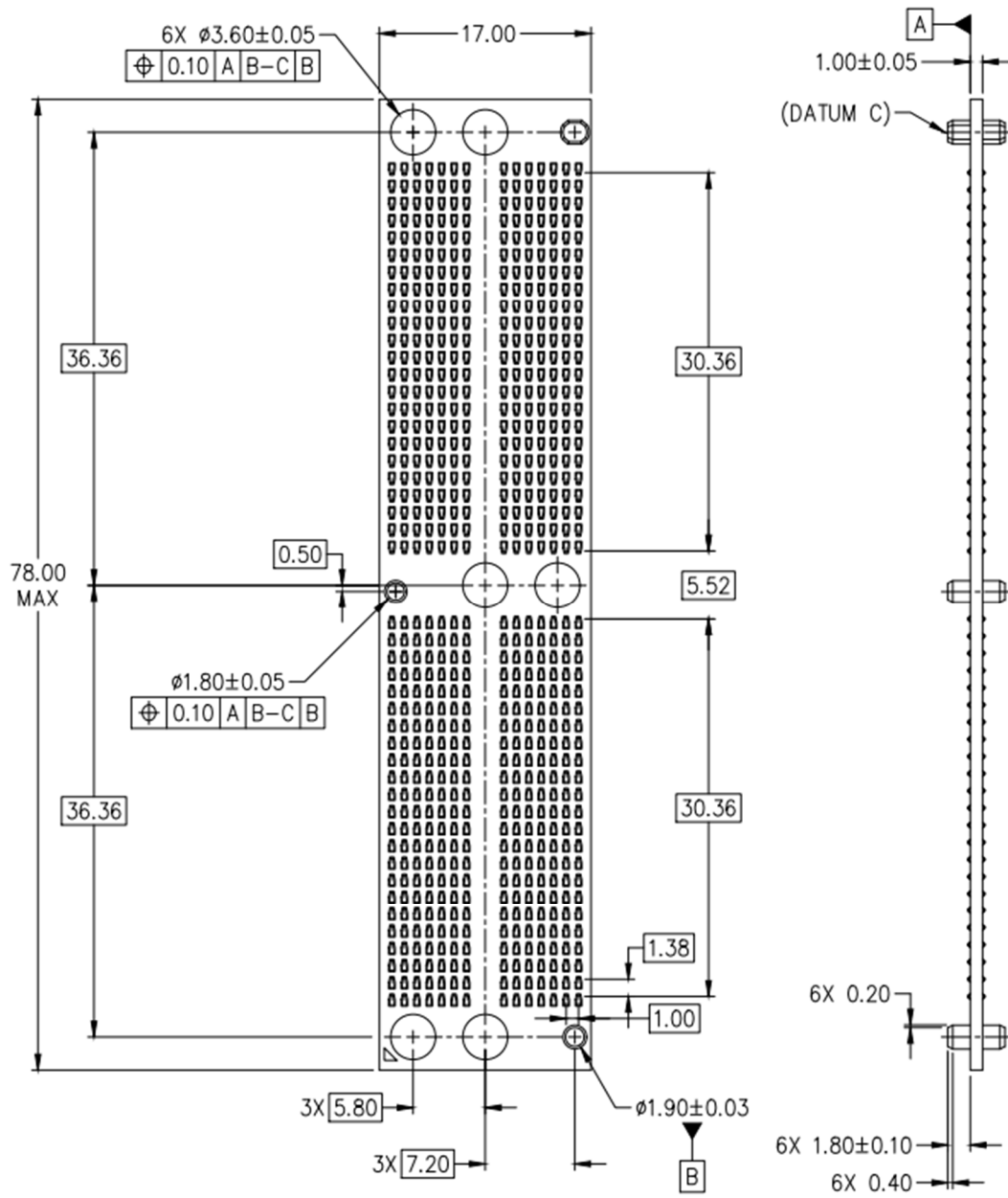


Figure 3 LPDDR5 CAMM2 Connector Socket Outline

For the detailed outline, refer to JEDEC JEP95, MO-357.



6.2 Reference top cover

To mitigate the LPDDR5 radiation impact on the proximity wireless device, such as Wi-Fi antenna. An optional top cover can be placed over the CAMM2 module. The top cover is also used as a top plate for structure enforcement and heat spread for thermal dissipation.

The reference top cover is shown in Figure 5 . The detail of a reference design is shown in Appendix E
A reference exposed GND strip along the edge on the top side of CAMM2 module is shown in Figure 6.

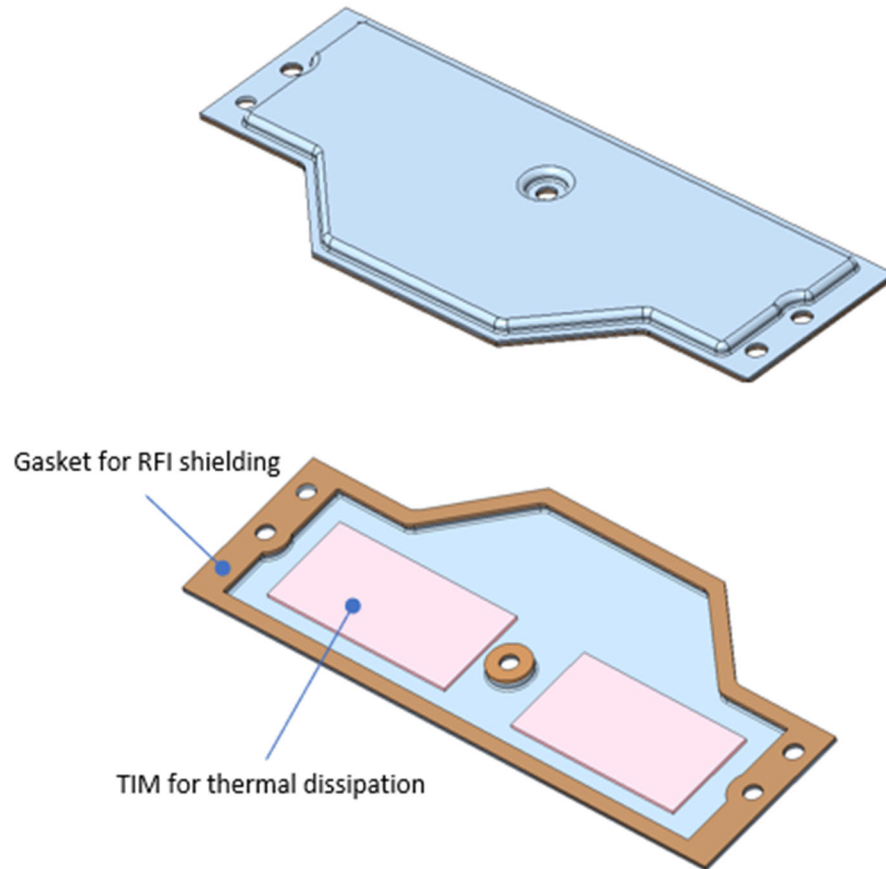
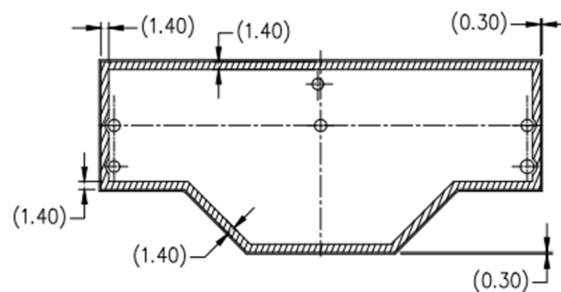


Figure 5 Reference top cover design



REFERENCE EXPOSED GND STRIP (BOTH SIDES)

Figure 6 Reference exposed GND strip for EMI/RFI shield

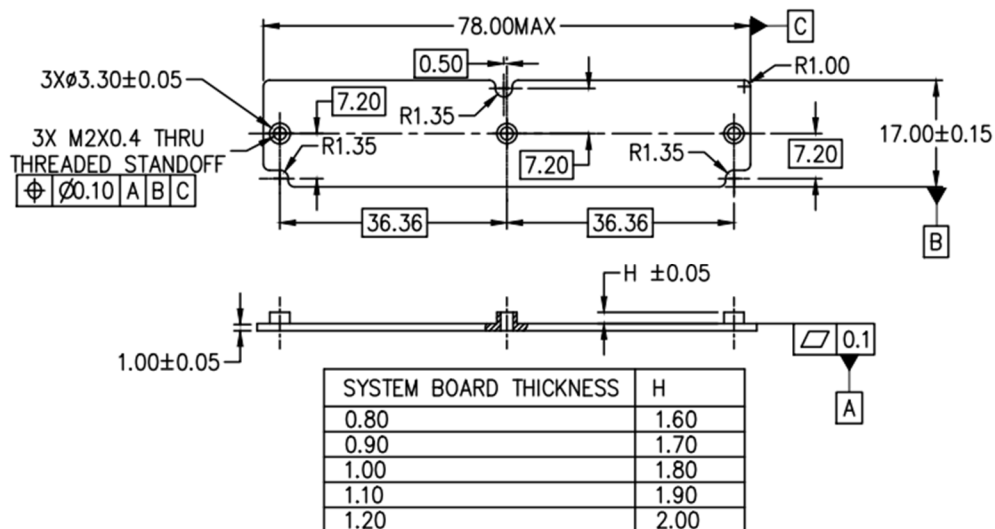


Figure 8 Reference backplate design

7.3 Reference assembly with top cover

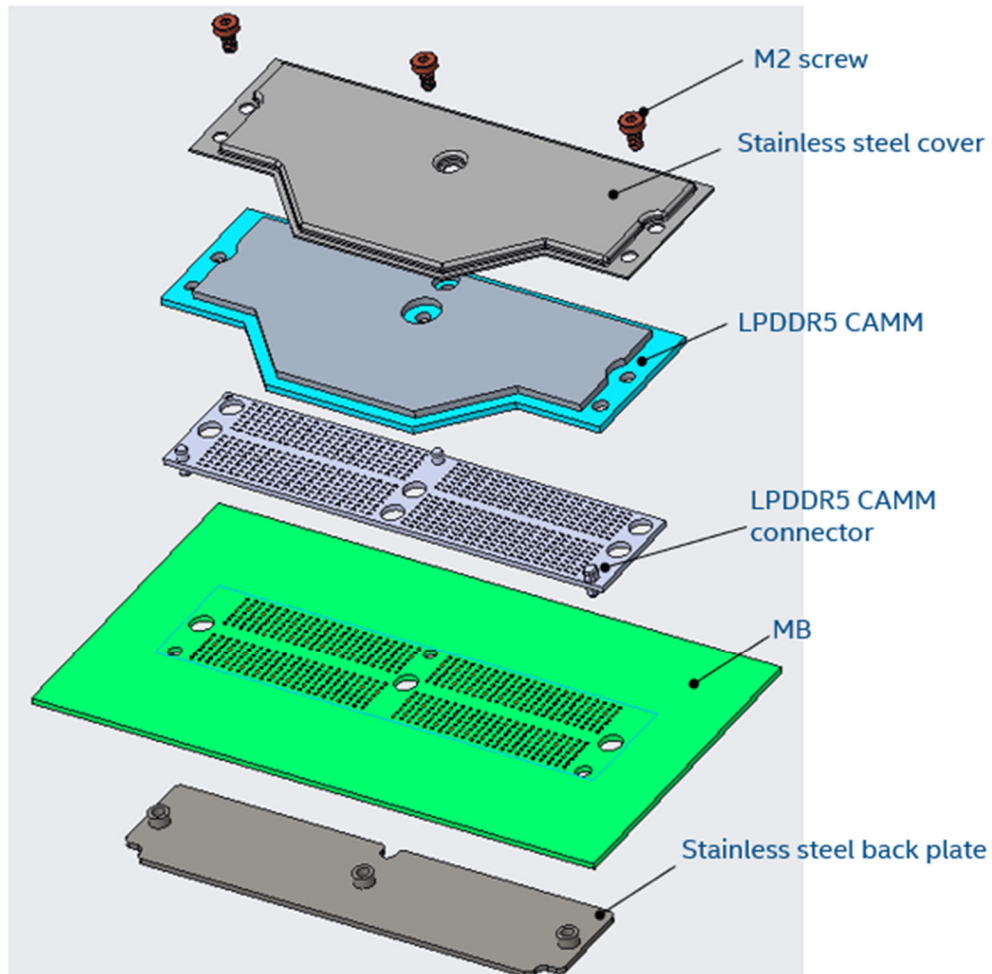


Figure 9 Reference backplate design

8 Shipping and handling tray

8.1 CAMM2 Connector Tray

Figure 7 depicts a reference shipping and handling tray for LPDDR5 CAMM2 connector.

For the detailed outline, refer to JEP95, CO-040

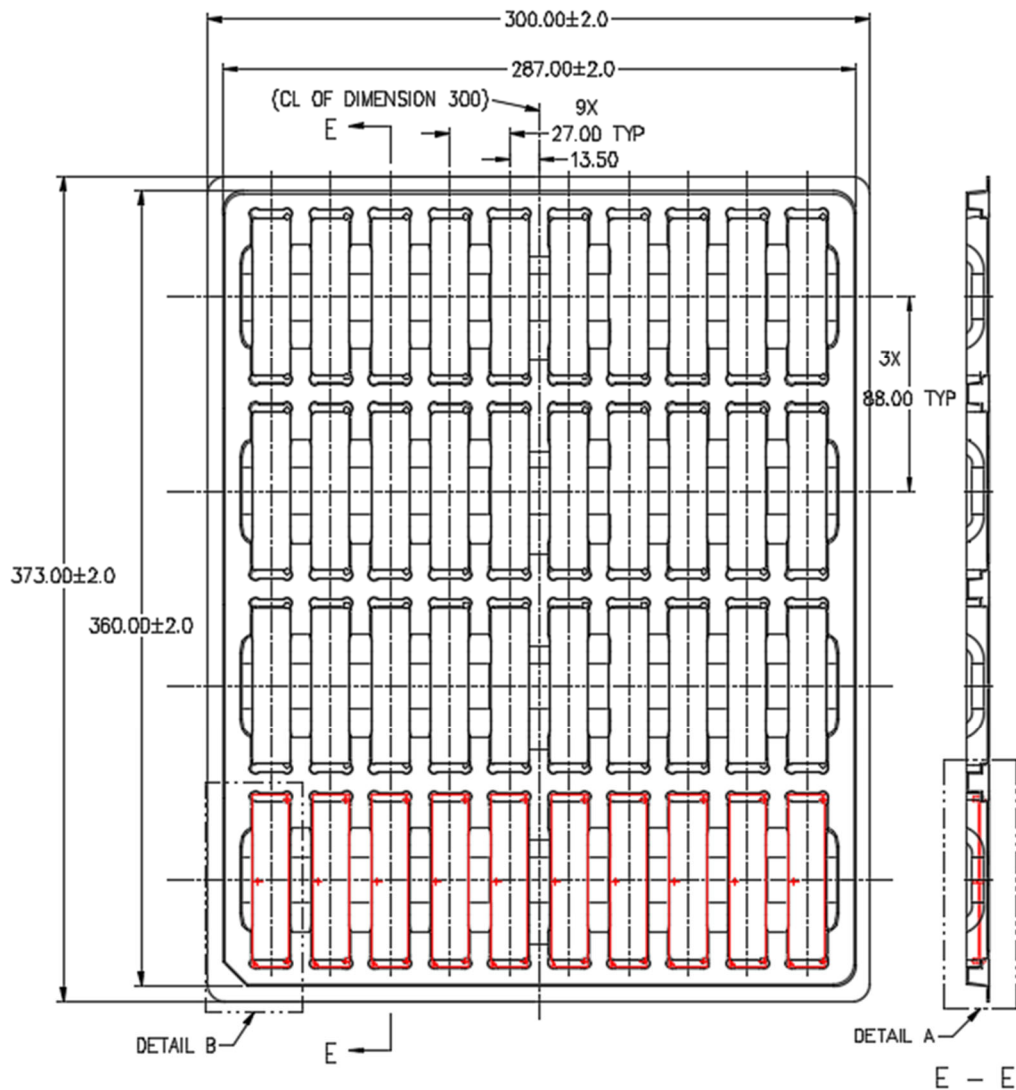


Figure 10 Reference tray for LPDDR5 CAMM2 connector

9 Performance requirements

Reliability benchmark testing shall be performed per EIA 364-1000 test groups 1, 2, 3, and 4 for 3, 5, or 7-year life cycle requirements. A minimum 5 samples are to be tested per subgroup.

9.1 Mechanical and other requirements

Table 2 - Mechanical and other requirements

Mechanical Test Description	Procedure	Requirement
Normal Force – Terminal (fully compressed)	EIA 364-29	Max 35 gf per pin
Retention Force – Terminal (optional)	EIA 364-29	50 gf minimum per pin; maximum movement of contact of 0.50 mm
Durability (mating/unmating)	EIA-364-09 Perform 25 cycles installation cycles	LLCR and no nickel plating exposed at contact interface
Additional Tests	Procedure	Requirement
Recommended fastening torque (mounting)		0.1~0.2 N.m (14.2~28.3 oz.in)
Recommended retention torque (un-mounting)		0.08 N.m. (11.3 oz.in) minimum
Module component reliability (optional)	IPC-TM-650 Dye and Pry	<25% solder joint crack

9.2 Reliability test conditions

Table 3 - Reliability test sequence

Test	Test Group			
	1	2	3	4
Low Level Contact Resistance	1,4,6	1,4,6,8	1,3,5,7	1,4,6,8,10
Reseating	5	7		9
Vibration			6	
Mechanical Shock			4	
Durability (preconditioning)	2	2	2	2
Temperature Life	3			
Temperature Life (preconditioning)				3
Thermal Shock		3		
Cyclic Temp and Humidity		5		
Mixed Flowing Gas				5
Thermal Disturbance				7
Retention torque (un-mounting)			8	
Dye and Pry			9	

9.3 Reliability test conditions (cont'd)

Table 4 - Reliability test conditions

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	EIA-364-09, perform 5 plug/unplug cycles	No evidence of physical damage
Temperature Life	EIA-364-17, Method A (without electrical load) 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 8	Electrical, mechanical, and environmental criteria
Temperature Life (preconditioning)	60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 9	
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Refer to Table 5.4.2
Shock Unpackaged	EIA-364 -27 Trapezoidal shock 50 g, $\pm 10\%$ Duration 11 ms Velocity change 170 inch/sec, $\pm 10\%$ Three drops in each of six directions are applied to each of the three samples Detail in Annex C	Electrical, mechanical, and environmental criteria
Vibration Unpackaged	EIA-364 -28 Random profile: 5 Hz @ 0.01 g ² /Hz to 20 Hz @ 0.02 g ² /Hz (slope up) 20 Hz to 500 Hz @ 0.02 g ² /Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Detail in Annex C	No discontinuities of ≥ 1 microsecond electrical, mechanical, and environmental criteria
Cyclic Temperature and Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition	Electrical, mechanical, and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 °C to 85 °C, perform 5 cycles in mated condition	Electrical, mechanical, and environmental criteria
Thermal Disturbance	EIA-364-1000 Cycle the connector between 15 ± 3 °C and 85 ± 3 °C, as measured on the part. Ramps should be a minimum of 2 °C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	Electrical, mechanical, and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per EIA 364-1000 Table 4.	Electrical, mechanical, and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

9.4 Environmental requirements

Table 5 - Connector environmental requirements

Environmental Requirements	Procedure	Requirement
Flammability	UL 94	V-0
Lead Free	RoHS compliant per IEC 62474	RoHS directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard (Clause 4)	Sample combustion followed by ion chromatography as specified in British Standard Methods BS EN 114582/2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

9.5 Electrical requirements

Table 6 - Connector electrical requirements

DC Electrical Requirements	Procedure	Requirement
LLCR Contact resistance, Initial	EIA-364 -23 Detail in Annex A	50 mΩ Max
LLCR (Contact resistance)	EIA364-23B Subject mated contacts assembled in housing to 20 mV maximum voltage at 100 mA maximum current	Post Stress: the resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading shall not exceed 20 mΩ
Withstanding Voltage	EIA-364-20, Condition I. 500 V ac at sea level.	One minute hold with no breakdown or flashover.
Insulation resistance	EIA-364 -21	1M Ω minimum
Current carrying capability at 30 °C temperature rise per contact	EIA-364 Test Procedure 70 Detail in Annex B	1.0 amp/pin

10 Signal Integrity requirements

The signal integrity requirements are measured by the connector and its interfaces with baseboard and module. The device under test (DUT) includes short stripline on baseboard, a $\varnothing 0.25$ mm micro-via, short trace between via to pad, pad on baseboard, connector pin, pad on module, short trace between pad to via, $\varnothing 0.25$ mm micro-via, and short stripline on module. The detail of the DUT is shown in Figure 11 and the detail of the testboard is described in Annex D.

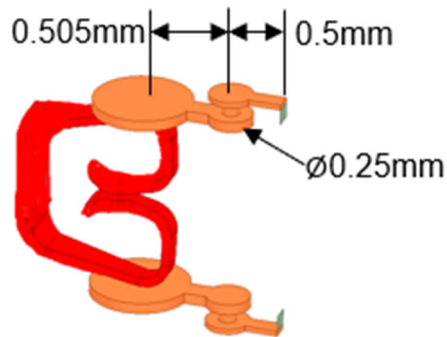


Figure 11: Device under test (DUT)

10.1 Frequency domain requirements

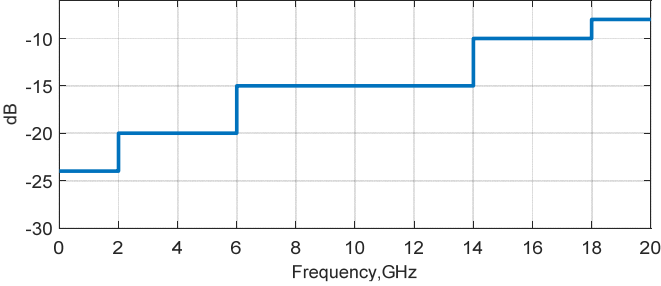
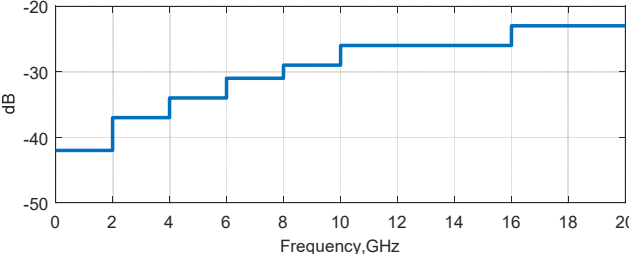
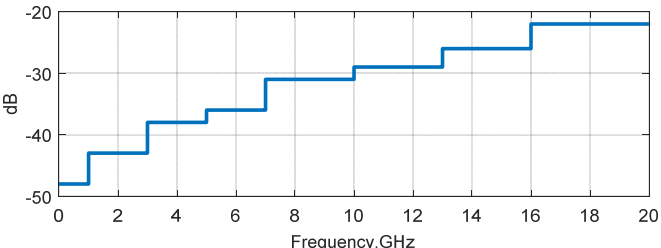
The S-parameter requirements for LPDDR5 CAMM2 connector are shown in Table 7.

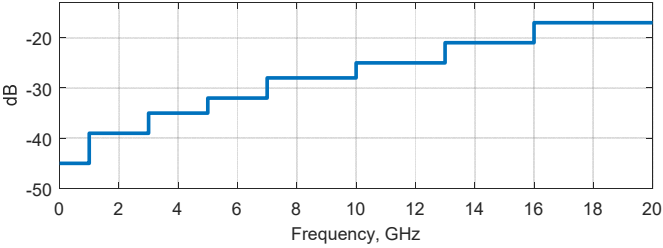
Notes:

- Effects of the baseboard pad, CAMM2 pad and micron via are included
- Reference impedance = 40 ohm

Table 7 - S-parameter requirements

S-Parameter	Target Value
Insertion Loss (IL) <u>Note:</u> <ul style="list-style-type: none"> • Measure from both the baseboard side and module side 	<p> > -0.30 dB ($f \leq 3.0$ GHz) > -0.40 dB ($3.0 \text{ GHz} < f \leq 8.0$ GHz) > -0.50 dB ($8.0 \text{ GHz} < f \leq 10.0$ GHz) > -0.80 dB ($10.0 \text{ GHz} < f \leq 14.0$ GHz) > -1.20dB ($14.0 \text{ GHz} < f \leq 17.0$ GHz) > -2.00 dB ($17.0 \text{ GHz} < f \leq 20.0$ GHz) </p>

<p>Return Loss (RL)</p> <p>Note:</p> <ul style="list-style-type: none"> • Signals with 1:1 S/G • Measure from both the baseboard side and module side 	<p>< -24.0 dB ($f \leq 2.0$ GHz)</p> <p>< -20.0 dB ($2.0 \text{ GHz} < f \leq 6.0$ GHz)</p> <p>< -15.0 dB ($6.0 \text{ GHz} < f \leq 14.0$ GHz)</p> <p>< -10.0 dB ($14.0 \text{ GHz} < f \leq 18.0$ GHz)</p> <p>< -8.0 dB ($18.0 \text{ GHz} < f \leq 20.0$ GHz)</p> 
<p>Near End Crosstalk (NEXT)</p> <p>Note:</p> <ul style="list-style-type: none"> • Both the victim and the aggressor are located at the same side • Measure from the baseboard side 	<p>< -42.0 dB ($f \leq 2.0$ GHz)</p> <p>< -37.0 dB ($2.0 \text{ GHz} < f \leq 4.0$ GHz)</p> <p>< -34.0 dB ($4.0 \text{ GHz} < f \leq 6.0$ GHz)</p> <p>< -31.0 dB ($6.0 \text{ GHz} < f \leq 8.0$ GHz)</p> <p>< -29.0 dB ($8.0 \text{ GHz} < f \leq 10.0$ GHz)</p> <p>< -26.0 dB ($10.0 \text{ GHz} < f \leq 16.0$ GHz)</p> <p>< -23.0 dB ($16.0 \text{ GHz} < f \leq 20.0$ GHz)</p> 
<p>Far End Crosstalk (FEXT)</p> <p>Note:</p> <ul style="list-style-type: none"> • Both the victim and the aggressor are located at the same side • Measure from the module side 	<p>< -48.0 dB ($f \leq 1.0$ GHz)</p> <p>< -43.0 dB ($1.0 \text{ GHz} < f \leq 3.0$ GHz)</p> <p>< -38.0 dB ($3.0 \text{ GHz} < f \leq 5.0$ GHz)</p> <p>< -36.0 dB ($5.0 \text{ GHz} < f \leq 7.0$ GHz)</p> <p>< -31.0 dB ($7.0 \text{ GHz} < f \leq 10.0$ GHz)</p> <p>< -29.0 dB ($10.0 \text{ GHz} < f \leq 13.0$ GHz)</p> <p>< -26.0 dB ($13.0 \text{ GHz} < f \leq 16.0$ GHz)</p> <p>< -22.0 dB ($16.0 \text{ GHz} < f \leq 20.0$ GHz)</p> 

<p>PSFEXT</p> <p>Note:</p> <ul style="list-style-type: none"> Measure from both the baseboard side and module side 	<p>< -45.0 dB ($f \leq 1.0$ GHz)</p> <p>< -39.0 dB ($1.0 \text{ GHz} < f \leq 3.0$ GHz)</p> <p>< -35.0 dB ($3.0 \text{ GHz} < f \leq 5.0$ GHz)</p> <p>< -32.0 dB ($5.0 \text{ GHz} < f \leq 7.0$ GHz)</p> <p>< -28.0 dB ($7.0 \text{ GHz} < f \leq 10.0$ GHz)</p> <p>< -25.0 dB ($10.0 \text{ GHz} < f \leq 13.0$ GHz)</p> <p>< -21.0 dB ($13.0 \text{ GHz} < f \leq 16.0$ GHz)</p> <p>< -17.0 dB ($16.0 \text{ GHz} < f \leq 20.0$ GHz)</p>  <table border="1"> <caption>Data points for the Return Loss Requirement Graph</caption> <thead> <tr> <th>Frequency Range (GHz)</th> <th>Return Loss Requirement (dB)</th> </tr> </thead> <tbody> <tr> <td>0 - 1.0</td> <td>< -45.0</td> </tr> <tr> <td>1.0 - 3.0</td> <td>< -39.0</td> </tr> <tr> <td>3.0 - 5.0</td> <td>< -35.0</td> </tr> <tr> <td>5.0 - 7.0</td> <td>< -32.0</td> </tr> <tr> <td>7.0 - 10.0</td> <td>< -28.0</td> </tr> <tr> <td>10.0 - 13.0</td> <td>< -25.0</td> </tr> <tr> <td>13.0 - 16.0</td> <td>< -21.0</td> </tr> <tr> <td>16.0 - 20.0</td> <td>< -17.0</td> </tr> </tbody> </table>	Frequency Range (GHz)	Return Loss Requirement (dB)	0 - 1.0	< -45.0	1.0 - 3.0	< -39.0	3.0 - 5.0	< -35.0	5.0 - 7.0	< -32.0	7.0 - 10.0	< -28.0	10.0 - 13.0	< -25.0	13.0 - 16.0	< -21.0	16.0 - 20.0	< -17.0
Frequency Range (GHz)	Return Loss Requirement (dB)																		
0 - 1.0	< -45.0																		
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3.0 - 5.0	< -35.0																		
5.0 - 7.0	< -32.0																		
7.0 - 10.0	< -28.0																		
10.0 - 13.0	< -25.0																		
13.0 - 16.0	< -21.0																		
16.0 - 20.0	< -17.0																		

10.2 Time domain requirements

The LPDDR5 CAMM2 connector impedance requirement is shown in Table 8.

Notes:

- Reference impedance = 50ohm
- Rise time: 40 ps (10%~90%) at reference plane.
- TDR launch is from both baseboard side and module side

Table 8 - Connector time domain requirement

Specification	Pass Criteria
Impedance	40~45 Ω

Annex A (informative) LLCR Measurements

A.1 Reference equipment

- Micro-ohmmeter (such as Keithly 580; Keysight/Agilent 4338B)
- Cable with clammer or pogo pins

A.2 4-wire measurement

Figure A.1 illustrates 4 wire LLCR measurement.

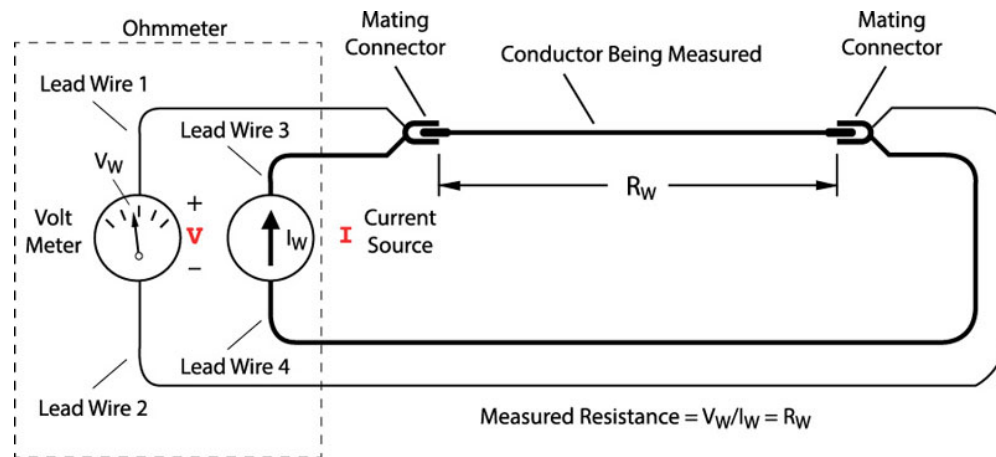


Figure A.1 — 4-wire measurement

A.2 Test fixture example

Figure A.2 and Figure A.3 illustrate LLCR measurement examples using 4-wire measurement.

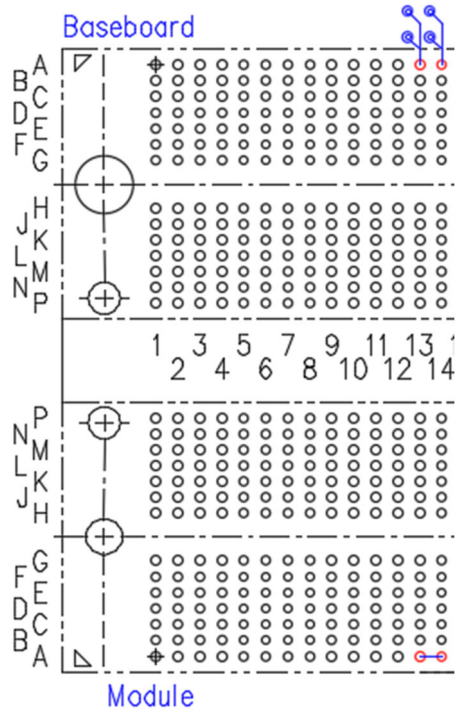


Figure A.1 — 4-wire connection example (2 pins in series)

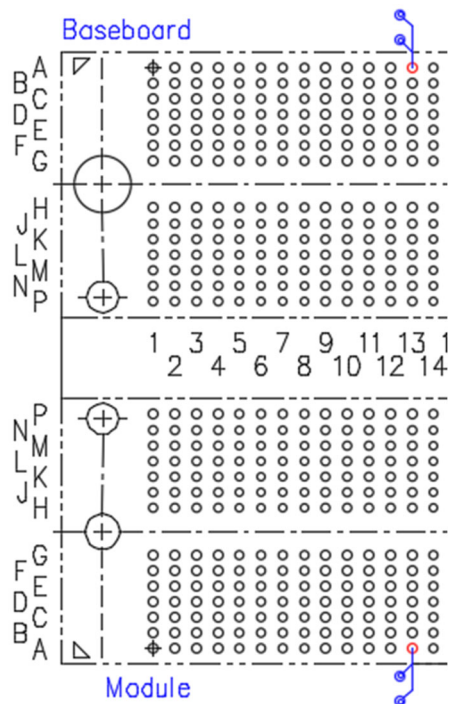


Figure A.2 — 4-wire connection example (single pin)

Annex B (informative) Current Carrying Capability Testing

B.1 Reference equipment

T-Rise Method (Reference EIA 364-70 Method 2)

B.2 Test procedure

The method is summarized as follows: Minimum of 5 connector samples.

- Ambient system temperature stabilized (testing to occur at ambient system temperature)
 - Current necessary to produce the specified temperature of 30C. (Do not exceed maximum connector temperature rating e.g. 105C)
 - Test multiple contacts (F23, G23, N23, P23, F24, G24, N24, P24) in housing per wiring diagram (current through wire 1 and wire 2).
- Report results per EIA 364-70 table “test documentation Annex”.

B.3 Test board daisy chain connection

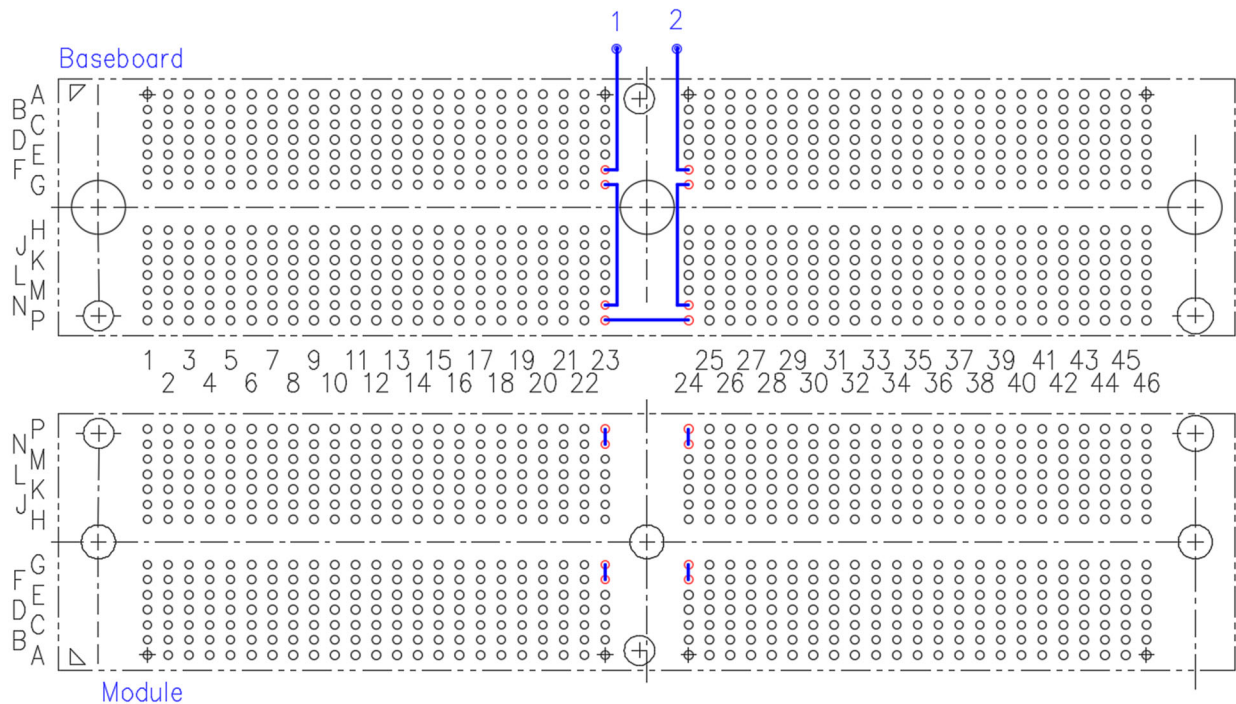


Figure B.1 — Daisy chain connection

Annex C (informative) Shock and vibration test board

C.1 Shock and vibration

Shock and vibration base board to be specified by OEM/ODM due to various system layouts.

C.2 Test Module - weight and center of gravity

- Module weight: 15 grams.
- Top cover weight: 10 grams
- Module shape: Follow MO-357 on module size and form factor.
- Center of gravity of module: 15 mm from the module straight edge.
- Module thickness: 1.20 +0/-0.10 mm.
- Module to check connector continuity and DRAM solder joint reliability.

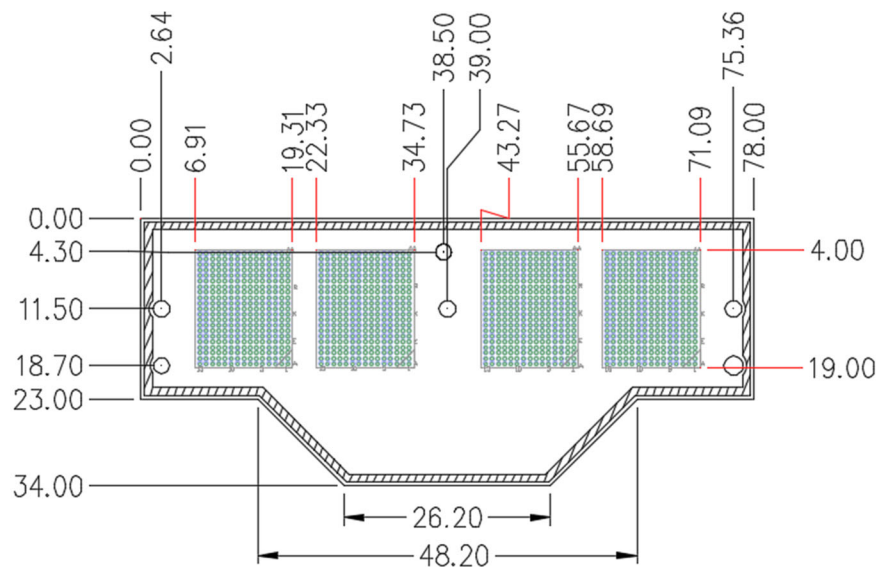


Figure C.1 —Example of the test module with DRAM location

C.3 Shock unpackaged

C.3.1 Purpose

To ensure the boards are sufficiently robust to withstand shocks when shipped in a system. Board un-packaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.3.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.3.3 Test Conditions

- Trapezoidal shock 50 g \pm 10%.

- Velocity change 170 inch/sec, $\pm 10\%$.
- Three drops in each of six directions are applied to each of the three samples.

C.4 Vibration unpackaged

C.4.1 Purpose

To ensure the board is sufficiently robust to withstand vibration when mounted in a system, which is being shipped. Board unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.4.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.4.3 Test Conditions

Random profile:

- 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up)
- 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat)
- Input acceleration is 3.13 g RMS
- 10 minutes per axis for all 3 axes on all samples
- Random control limit tolerance is ± 3 dB

Annex D (informative) Signal integrity test board

D.1 Reference Equipment

Vector Network Analyzer (VNA) System

2X through calibration capability required.

Connectors: Molex 2.92mm connector (# 0732520090) or equivalent connector

Two 50 Ω high frequency, low loss phase-matched cables. Recommended cables are offered by Micro Coax (part number UFB197C) or equivalence. The cables are used to connect the 2.92mm connector to the measurement ports on the VNA.

D.2 Test board

The testboard includes base board and module card. 2X through calibration traces are included on the base board to save PCB space. There is 1X through trace on base board as well for rise time setup for TDR impedance measurement.

D.2.1 Test board stackup

Figure D.1 describe details of the 6-layer DUT board and DUT module PCB stackup to be used. The DUT board and DUT module impedance are defined as 50 ($\pm 5\%$) ohms, recommended trace width for the testboard is 6.5 mil.

		THICKNESS	MATERIAL TYPE
LAYER 1 (PLATED 1/2oz Cu)		.06096	H-VSP
		.089	TUC TU883
LAYER 2 (GND 1/2oz Cu)		.03048	H-VSP
		.30	TUC TU883
LAYER 3 (GND 1/2 oz Cu)		.03048	RTF
		.2020	TUC TU883
LAYER 4 (GND 1/2 oz Cu)		.03048	RTF
		.30	TUC TU883
LAYER 5 (GND 1/2 oz Cu)		.03048	H-VSP
		.089	TUC TU883
LAYER 6 (PLATED 1/2oz Cu)		.06096	H-VSP
	TOTAL	1.2mm	+0.12 -0.12

Figure D.1 Stackup of CAMM2 connector testboard

D.3.2 Baseboard and CAMM2

The reference plane for deembeded is set to be 0.5 mm from micro-via pad on L2. The trace length from reference plane to 2.92mm connector is 19.5 mm.

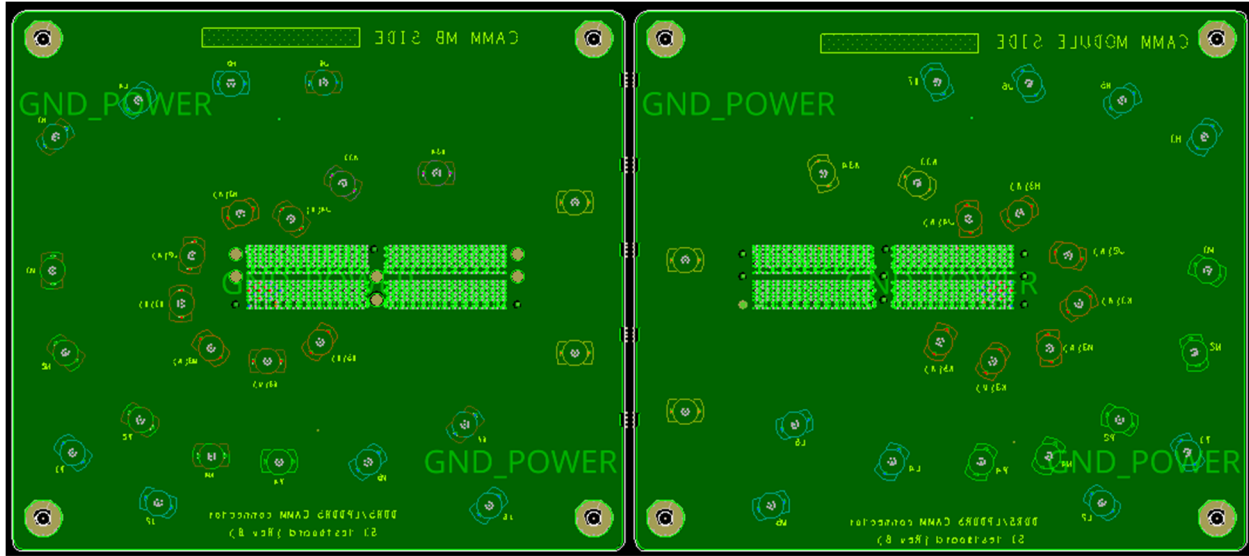


Figure D.2 CAMM2 base board

D.3.4 2.92mm connector

Molex 2.92mm connector (# 0732520090) or equivalence is recommended to use, as shown in Figure D.4. The 2.92mm connector will be screw mounted on the PCB for cable vertical access.

A low profile 0-80 screw (screw head <0.9mm) is used to fasten the 2.92mm connector on the board to avoid any interference during CAMM2 testboard assembly.

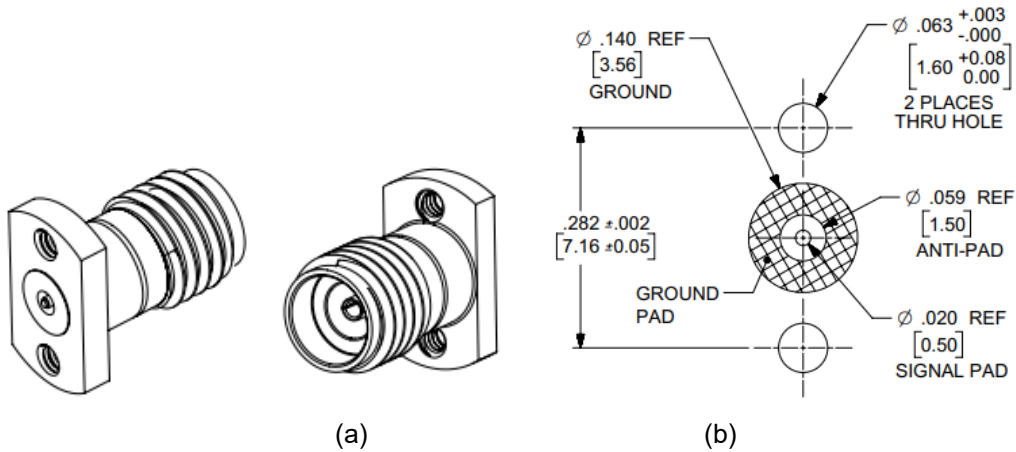


Figure D.3 (a) 2.92mm connector (b) Recommended footprint of the 2.92mm connector

D.4 Testing

Any 2.92mm connectors not connected to VNA for testing should be terminated with 50-ohm load.

D. 5 Data processing

The pins used for testing include K1, J2, H3, K3, M3, J4 and K5. K3, J2 are selected as the victim for single pin near end crosstalk and far end crosstalk calculations. K3 is selected as victim for power sum far end crosstalk calculation.

	1	2	3	4	5	6
H	PWR_GOO	VSS	DQ	VSS	LPDDR0_CS	VSS
J	VSS	DQ	VSS	DQ	VSS	DQ
K	DQ	VSS	DQ	VSS	DQ	VSS
L	VSS	DQ	VSS	DQ	VSS	DQ
M	DQ	VSS	DM	VSS	DQ	VSS
N	VSS	DQS_P	VSS	WCK_P	VSS	WCK_P
P	PWR_EN	DQS_N	VSS	DCK_N	VSS	DCK_N

Figure D.4 Pins selected for testing

- Impedance: All 7 DQ pins
- Insertion loss: All 7 DQ pins
- Return loss: All 7 DQ pins
- NEXT: 1) K3 as victim, the rest 6 pins as aggressors 2) J2 as victim, K1, H3 as aggressors
- FEXT: 1) K3 as victim, the rest 6 pins as aggressors 2) J2 as victim, K1, H3 as aggressors
- PSFEXT: K3 as victim. The rest 6 pins as aggressors, pin J2 and pin J4 to be counted twice (to cover L2 and L4 which are not tested)

D.6 Power Sum crosstalk

The power sum far end crosstalk (PSFEXT) is calculated from the individual FEXT aggressors. PSFEXT is computed as shown in Figure A.5, where $FEXT_n$ is the crosstalk, in dB, of aggressor n.

$$PSFEXT = 10 \cdot \log_{10} \left(\sum_{n=1}^N 10^{\frac{FEXT_n}{10}} \right)$$

Figure D.5 PSFEXT calculation

D. 7 Impedance

The structure of the DUT is short. The testboard impedance and the rise time will impact the DUT impedance. the DUT impedance is reading as the low value of profile, as shown in Figure D.6

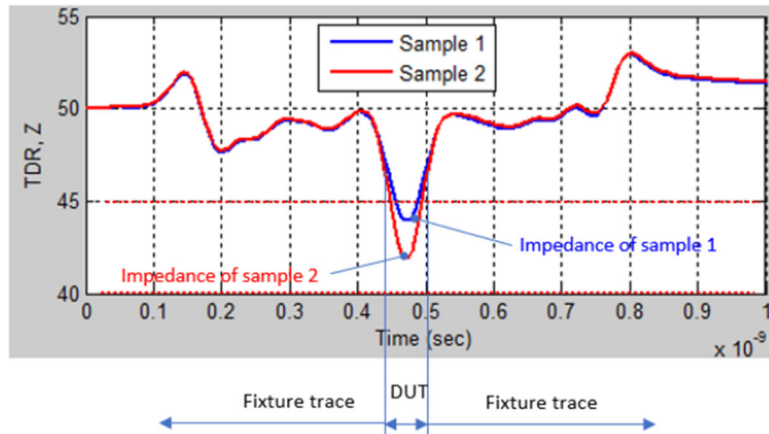
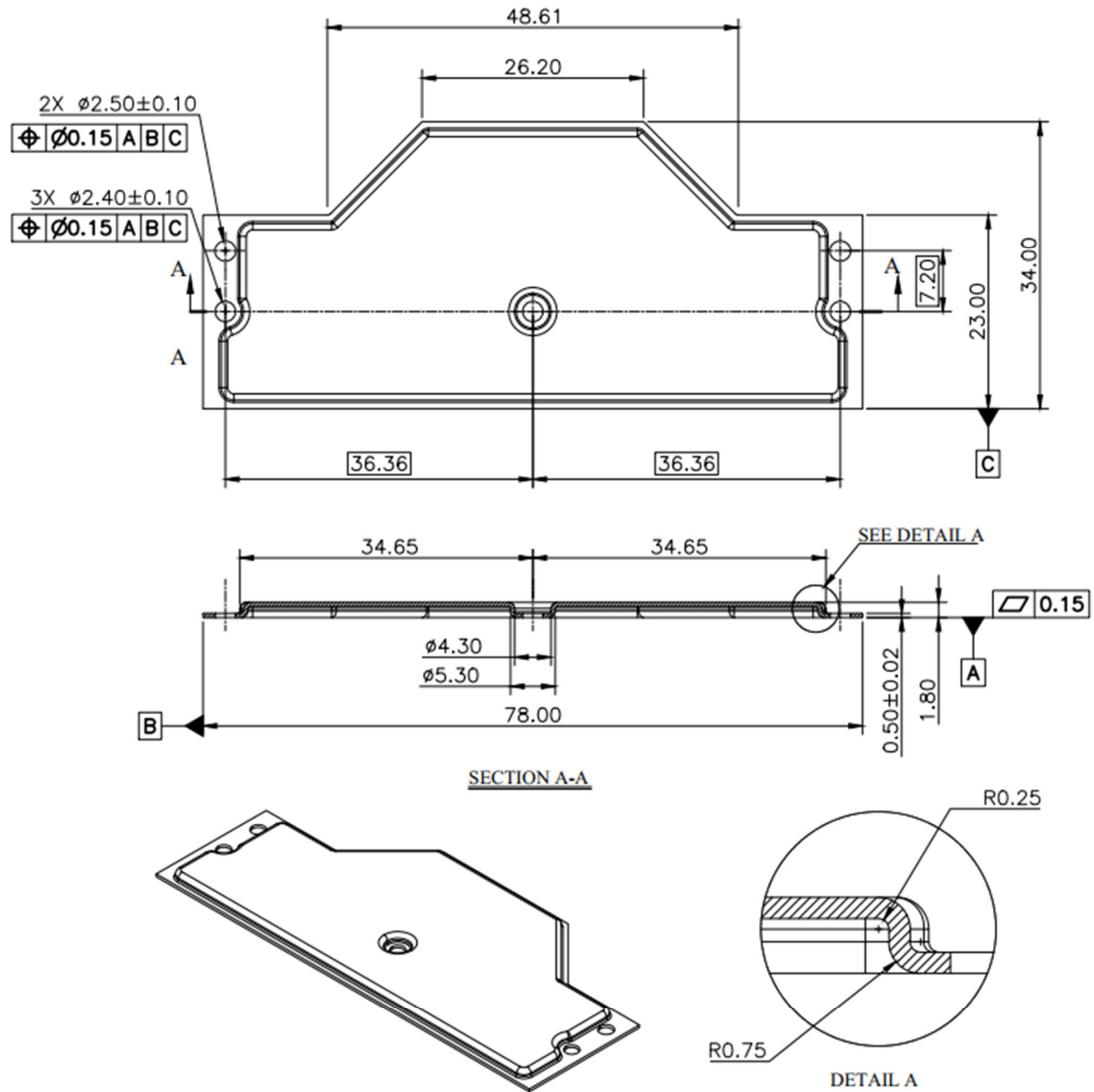


Figure D.6 Impedance of the DUT

Annex E (informative) Top cover design



NOTES:

1. MATERIAL SPECIFICATION: STAINLESS STEEL
2. TOLERANCES ON ALL DIMENSIONS ± 0.15 UNLESS OTHERWISE SPECIFIED.
3. ALL DIMENSIONS ARE MM.
4. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009.
5. REFER TO MO-357 TO ENSURE NO INTERFERENCE RISK WITH COMPONENTS ON MODULE DURING THE ASSEMBLY.

Figure E.1 Reference cover design

TASK GROUP CONTRIBUTOR

ALIBABA GROUP(U.S.) INC.
AMPHENOL CORPORATION
ARGOSY RESEARCH INC.
CHANGXIN MEMORY TECHNOLOGIES INC. (CXMT)
DELL INC.
FOXCONN INTERCONNECT TECHNOLOGY LTD
HEWLETT PACKARD ENTERPRISE COMPANY
HP INC.
INTEL CORPORATION
LENOVO
LOTES CO. LTD.
LUXSHARE-ICT, INC.
MICRON TECHNOLOGY INC.
MOLEX LLC
SAMSUNG SEMICONDUCTOR
SHENZHEN DEREN ELECTRONIC CO. LTD.
SK HYNIX INC.
TE CONNECTIVITY
WLCO SHENZHEN CO. LTD.

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INITIAL ISSUE: A	DATE: JULY 2024	ITEM NUMBER: 11.14-225A
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ISSUE:	DATE:	ITEM NUMBER:
LOCATION:	CHANGED FROM:	CHANGED TO: